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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,688	11/18/2003	Peter A. Sandon	END920030075US1	4804

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SCHMEISER, OLSEN & WATTS
22 CENTURY HILL DRIVE
SUITE 302
LATHAM, NY 12110

EXAMINER	
JOHNSON, BRIAN P	
ART UNIT	**PAPER NUMBER**
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/715,688	SANDON ET AL.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-7,11-14,16-19,21-23 and 26-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,4-7,11-14,16-19 and 21-23* is/are allowed.

6)☒ Claim(s) *26-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1, 4-7, 11-14, 16-19, 21-23 and 26-32 have been examined.

Examiner acknowledges the receipt of claim amendments and remarks filed 26 March 2007.

Specification

The new title as amended is accepted; however, there appears to be an error with the amendment of the title. Examiner recommends changing the title to the original version once more.

Claim Objections

Objection is withdrawn in light of Applicant's amendments.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 26, 27, and 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook (U.S. Patent No. 5,812,147) in view of Gostin (U.S. Patent No. 5,832,290).

4. Regarding claim 26, Van Hook discloses a method for processing matrix data comprising: a processor (col 3 lines 42); M independent vector register files within the processor (fig. 2A), said M vector register files collectively storing the matrix of L data elements, each data element having B binary bits, said matrix having N rows and M columns, said L=N*M, each column having K subcolumns said N is greater than or equal to 2, said M is greater than or equal to 2, said K is greater than or equal to 1, said B is greater than or equal to one each row of said N rows being addressable, each subcolumn of said K subcolumns being addressable said matrix including a set of arrays such that each array is a row or subcolumn of the matrix, and

Executing an instruction by said processor, said instruction performing an operation on a first array or the set of arrays, said operation being performed with selectivity with respect to data elements of the first array (col 2 lines 24-28); and

Van Hook fails to disclose that a hardware multiplexer is used to control the vector processor.

Gostin discloses a vector register file controlled by the multiplexer (col 5 lines 1-5).

Van Hook, a computing system with a large variety of ways to access it's register file, would be clearly motivated to use a simple, fast, and widely tested technique for using a common multiplexer to control its vector register file.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the vector register file of Van Hook to utilize a multiplexer of Gostin. Examiner takes Official Notice that a very simple and fast multiplexer would include a binary switch to output binary values.

5. Regarding claims 27, 29, 30, 31 and 32, Van Hook/Gostin discloses the limitations of claim 26:

6. Regarding claim 27, Van Hook discloses the processor of claims 26, wherein the processor further comprises M address registers, wherein each address register of the M address registers is associated with a corresponding one of the M vector register files,

Wherein each of the M vector register files includes an array of N registers, wherein each of the N*M registers of the M vector register files are adapted to store a data element of the L data elements (fig 2A), and wherein each vector register file is independently addressable through its associated address register being adapted to point to one of the N registers of said vector register file (col 4 lines 41-55).

7. Regarding claim 29, Van Hook/Gostin discloses the processor of claim 26, wherein the instruction is adapted to rearrange the data elements of the first array within the first array.

Examiner asserts that a vector register file, like the one disclosed in Van Hook, is clearly able to rearrange its data.

8. Regarding claim 30, Van Hook/Gostin discloses the processor of claims 26, wherein the processor is not adapted to duplicatively store the L data elements.

9. Regarding claim 31, Van Hook/Gostin discloses the method of claim 26, said K is more than equal to 2 and N = K*M.

10. Regarding claim 32, Van Hook/Gostin discloses the method of claim 26, wherein each multiplexer of the M multiplexers comprises a set of binary switches subject to each binary switch being on or off and respectively represented by a binary bit 1 or 0 such that the value of the multiplexer consists of the composite value of the binary bits.

11. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook/Gostin in view of AMD 64-bit Technology (herein AMD).

12. Regarding claim 28, Van Hook/Gostins discloses the processor of claim 26 and the use of instructions utilizing the memory matrix (fig 2A).

Van Hook/Gostin fails to disclose enough detail about the types of instructions used.

AMD discloses a vector-shift instruction being supported (page 135 last paragraph, second to last line) and a vector move instruction (page 137 section 4.2.5 first paragraph).

It is expected that one of ordinary skill in the art would have realized the advantages of utilizing a shift and move instruction. Both of these instructions are fairly standard in most instruction sets because they give the programmer the ability to rearrange and interchange vector registers in a single instruction, steps that are often times essential while programming software to be utilized on a processor. AMD even discloses that "Move instructions...are among the most frequently used instructions in 128-bit media procedures" (page 137 section 4.2.5 first three lines). Examiner asserts that shift instructions are also commonly utilized by programmers. For these reasons, Lawrie would be motivated to include these instructions in the instruction set of the referenced invention.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the processing system of Van Hook to include vector-move and vector-shift instructions in order to have instructions that "insert an exact copy of the first array into the second array" and "rearrange the data elements of the first array within the first array", respectively.

Maintained Rejections

Claims 26, 27 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Access and Alignment of Data in an Array Processor (herein Lawrie).

13. Regarding claim 26, Lawrie discloses a processor, comprising M independent vector register files (page 99 introduction paragraph 1), said M vector register files adapted to collectively store a matrix of L data elements (page 99 section II second paragraph), each data element having B binary bits, said matrix having N rows and M columns, said L=N*M (page 99 section II second paragraph line 3), each column having K subcolumns (page 108 lines 11-14), said N.gtoreq.2, said M.gtoreq.2 (page 99 section II second paragraph line 3), said K.gtoreq.1, said B.gtoreq.1, each row of said N rows being addressable (page 99 section II second paragraph lines 4-6), each subcolumn of said K subcolumns being addressable (page 108 lines 11-14),

Said matrix including a set of arrays such that each array is a row or subcolumn of the matrix (fig 2), said processor adapted to execute an instruction that performs an operation on a first array of the set of arrays, said operation being performed with selectivity with respect to the data elements of the first array (page 99 introduction paragraph 1).

Lawrie also discloses the processor of claims 26, wherein the processor further comprises M multiplexors respectively coupled to the M vector register files, and

wherein the values associated with the M multiplexors control said selectivity (page 100 col 1 second paragraph).

Note that, according to Wordnet ® 2.0 © 2003 Princeton University, a multiplexor is "a device that can interleave two or more activities"; therefore, the mechanism used to choose what values are put into the register file, a mechanism that must

14. Regarding claim 27, Lawrie discloses the processor of claim 26, wherein the processor further comprises M address registers (page 99 and 100 section II), wherein each address register of the M address registers is associated with a corresponding one of the M vector register files (page 108 lines 11-14),

Note that the rows are accessible, suggesting they are addressable, further suggesting that there is an "address register" for each register file (or row).

Wherein each of the M vector register files includes an array of N registers (page 99 and 100 section II), wherein each of the N*M registers of the M vector register files are adapted to store a data element of the L data elements (page 99 and 100 section II), and wherein each vector register file is independently addressable through its associated address register being adapted to point to one of the N registers of said vector register file (page 108 lines 11-14).

15. Regarding claim 30, Lawrie discloses the processor of claim 26, wherein the processor is not adapted to duplicatively store the L data elements (page 100 fig 2).

16. Claims 28 and 29 rejected under 35 U.S.C. 103(a) as being unpatentable over Lawrie in view of AMD 64-bit Technology (herein AMD).

Regarding claims 28, Lawrie discloses the processor of claim 26 and the use of instructions utilizing the memory matrix (page 99 introduction).

Lawrie fails to disclose enough detail about the types of instructions used.

AMD discloses a vector-shift instruction being supported (page 135 last paragraph, second to last line) and a vector move instruction (page 137 section 4.2.5 first paragraph).

It is expected that one of ordinary skill in the art would have realized the advantages of utilizing a shift and move instruction. Both of these instructions are fairly standard in most instruction sets because they give the programmer the ability to rearrange and interchange vector registers in a single instruction, steps that are often times essential while programming software to be utilized on a processor. AMD even discloses that "Move instructions...are among the most frequently used instructions in 128-bit media procedures" (page 137 section 4.2.5 first three lines). Examiner asserts that shift instructions are also commonly utilized by programmers. For these reasons, Lawrie would be motivated to include these instructions in the instruction set of the referenced invention.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the processing system of Lawrie to include vector-move and vector-shift instructions in order to have instructions that "insert an exact copy of the first array into

the second array" and "rearrange the data elements of the first array within the first array", respectively.

Allowable Subject Matter

17. Claims 1, 4-7, 11-14, 16-19, 21-23 allowed. Applicant's arguments with respect to the independent claims are persuasive.

Response to Arguments

18. Applicant's arguments filed 26 March 2007 have been fully considered but they are not persuasive.

19. Applicant states:

"As applied to claim 26, Applicants assert that it does not necessarily and inevitably follow from the teachings in Lawrie coupled with the Examiner's cited definition of 'multiplexor' that M multiplexors are respectively coupled to the M vector registers subject to M is greater than or equal to 2. First, a mechanism that determines the values to be put in a register file is not necessarily a device that interleaves two or more values. For example, an operation of copying a fixed array of values into a register file does not necessarily require utilization of a device that interleaves two or more values."

It is true that if Lawrie were limited to Applicant's example, a multiplexer would not be required, but this is not the case in Lawrie. See Introduction on page 99.

20. Applicant states:

"Second, even if it is inherent to have a device that interleaves two or more values in order to determine the values to be put in a register file, it is not inherent that M multiplexors are respectively coupled to the M vector registers such that M is greater than or equal to two. For example, using the Examiner's definition of "multiplexor", a single multiplexor (i.e., one device that interleaves two or more values) could be used to put in M register files such that M is greater than or equal to two. Thus, it does not necessarily and inevitably follow from the teachings in Lawrie that M multiplexors must be used to put values in M register files subject to M is greater than or equal to two"

Examiner disagrees. A large, multi-bit multiplexer is composed of multiple single-bit multiplexers.

21. Applicant states:

"Moreover, it does not necessarily and inevitably follow from the teachings in Lawrie that the values associated with M multiplexors must be used to control the claimed selectivity, since the selectivity can be controlled by either a single multiplexor or by a variety of other logic devices."

Examiner disagrees. If these "other logic devices" control the selectivity, then they are interpreted to be part of the multiplexer.

22. Applicant states:

"Applicants assert that the alleged motivation to modify Lawrie ("instruction that " insert an exact copy of the first array into the second array") teaches away from what is recited in claim 28 (wherein said copying does not insert an exact copy of the first array into the second array").

Examiner disagrees. Both of these options can be satisfied by different uses of the shift and move instructions.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100